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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte Yi-Hsien HAO, et al.

October 5, 2006

Serial No. 09/492,265
Appeal No.:
Group Art Unit: 2616

Enclosed is a check in the amount of Five Hundred Dollars ($500.00) to cover the official fee for this Appeal Brief. In the event that there may be any fees due with respect to the filing of this paper, please charge Deposit Account No. 50-2222.

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Appeal Brief (in triplicate)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Appellant:

Yi-Hsien HAO, et al. Appeal No.:

Serial Number: 09/492,265 Group Art Unit: 2616

Filed: January 27, 2000 Examiner: Philpott, Justin M.

For: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

BRIEF ON APPEAL

October 5, 2006

I. INTRODUCTION

This is an appeal from the final rejection set forth in an Official Action dated April 27, 2006, finally rejecting claims 1-60, all of the claims pending in this application, as being obvious over US Patent No. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), further in view of US Patent No. 5,860,136 to Fenner (Fenner), further in view of US Patent No, 6,614,796 to Black et al. (Black). A Request for Reconsideration was timely filed on June 27, 2006. An Advisory Action was issued on July 10, 2006, indicating that the request for reconsideration had been considered but did not place the application in condition for allowance. A Notice of Appeal and Pre-Appeal Brief Request for Review were timely filed on July 27, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review was issued on September 5, 2006, indicating that the application remains under appeal because there is at least one actual issue for appeal. This Appeal Brief is being timely filed.

II. REAL PARTY IN INTEREST

The real parties in interest in this application are Broadcom Corporation of Irvine, California, by virtue of an Assignment which was submitted for recordation on June 16, 2000 and which was recorded at Reel 012041, Frame 0772, on July 30, 2001.

III. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences which will directly effect or be directly effected by or have a bearing on the Board's decision in this appeal.

IV. STATUS OF CLAIMS

Claims 1-60, all of the claims pending in the present application are the subject of this appeal. Claims 1-60 stand rejected under 35 U.S.C. 103(a) as being obvious over US Patent No. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), further in view of US Patent No. 5,860,136 to Fenner (Fenner), further in view of US Patent No, 6,614,796 to Black et al. (Black). The PTO's rejections of claims 1-60 set forth in the Final Office Action dated April 27, 2006 is being appealed.

V. STATUS OF AMENDMENTS

The claims were last amended in the Response filed October 20, 2005. No amendments to the claims have been filed subsequent to the October 20, 2005 Response.

VI. SUMMARY OF THE INVENTION

The object of the invention is to enable a memory structure to resolve addresses in a packet-based network switch. Embodiments of the present invention enable bandwidth savings that are attributed to a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table.

Claim 1, from which claims 2-7 depend, recites a memory structure. See for example, Figure 1 elements 3-6 and page 4 line 30 – page 5 line 7. The memory structure includes an Address Resolution Table that resolves addresses in a packet-based network switch. See for example, Figure 1 elements 1 and 5 and page 4 line 30 – page 5 line 7. The memory structure uses a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. See for example, page 6 lines 20-29 and Figure 4 element 23. A Packet Storage Table is adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. See for example, Figure 1 elements 1 and 4 and page 4 line 35 – page 5 line1. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution

of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5. The entire packet is to be transmitted. See for example, page 7 lines 12-15.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure. See for example, Figure 1 elements 3-6 and page 4 line 30 – page 5 line 7. The memory structure includes an Address Resolution Table having an associative memory structure and uses a key to index a location within the Address Resolution Table. See for example Figure 1 elements 1 and 5, and page 4 line 30 – page 5 line 7, page 5 lines 24-29, and page 6 lines 20-29 and Figure 4 element 23. The Address Resolution Table resolves addresses in a packet-based network switch. See for example, Figure 1 elements 1 and 5 and page 4 line 30 – page 5 line 7. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12, and page 6 line 32 – page 7 line 5. The key is a predefined portion of a packet destination address. See for example, page 6 lines 20-29 and Figure 4 element 23.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. See for example Figure 1 elements 3 and 5, page 5 lines 21-24. The Address Resolution Table resolves addresses in a packet-based network switch by using a key to index a location within the Address Resolution Table. See for example, Figure 1 element 5, page 6 lines 20-29 and Figure 4 element 23. A

Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. See for example, Figure 1 element 6, page 10 lines 19-23. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. See for example Figure 1 element 4, page 10 lines 19-21. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key wherein the key is a predefined portion of a packet destination address. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5, page 6 lines 20-29 and Figure 4 element 23.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch. See for example Figure 1 element 1.

The packet-based switch includes a shared memory structure having an Address Resolution Table and a Packet Storage Table. See for example, Figure 1 elements 1, 4 and 5. A key indexes a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. See for example page 6 lines 20-29 and Figure 4 element 23. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5. The entire packet is to be transmitted. See for

example page 7 lines 12-15.

Claim 32, upon which claims 33-51 are dependent, recites a packet-based switch having a memory structure. See for example, Figure 1 elements 1 and 3, page 4 line 30 – page 5 line 10. The memory structure includes an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location with the Address Resolution Table. See for example Figure 1 elements 3 and 5, page 5 lines 21-24, page 6 lines 20-29. The key is a predefined portion of a packet destination address. See for example figure 4 element 22, page 8 lines 3-14. The memory structure includes a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value. See for example, Figure 1 element 6, page 10 lines 19-23. The memory structure includes a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. See for example Figure 1 elements 1 and 4 and page 4 line35 – page 5 line1. A single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5, page 8 lines 28-29. The entire packet is to be transmitted. See for example page 7 lines 12-15.

Claim 52, upon which claims 53-56 are dependent, recites a packet-based switch. See for example figure 1 element 1. The packet-based switch includes an Address

Resolution Table having a one-way associative memory structure. See for example Figure 1 element 5, page 5 lines 21-24. A key is used to index a location within the Address Resolution Table. See for example, page 6 lines 20-29. A Packet Data Buffer Table shares a memory block with an Address Resolution Table. See for example Figure 1 elements 3 and 4, page 4 line35 page 5 line 1.. A single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5, page 8 lines 28-29. The key is a predefined portion of a packet destination address, wherein the entire packet is to be transmitted. See for example figure 4 element 22, page 8 lines 3-14.

Claim 57, upon which claims 58-60 are dependent, recites a packet-based switch. See for example Figure 1 element 1. The packet-based switch includes an Address Resolution Table having a direct-mapped/one-way associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch. See for example Figure 1 element 5, page 5 lines 21-24. A key is used to index a location within the Address Resolution Table. See for example, page 6 lines 20-29. A single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. See for example, Figure 1 element 6, Figure 2 element 12 and page 6 line 32 – page 7 line 5, page 8 lines 28-29. The key is a predefined portion of a packet destination address. See for example figure 4 element 22, page 8 lines 3-14. The entire packet is to be

transmitted. See for example, page 7 lines 12-15.

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The PTO's rejection of claims 1-60 over US Patent No. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), further in view of US Patent No. 5,860,136 to Fenner (Fenner), further in view of US Patent No, 6,614,796 to Black et al. (Black) as set forth in the Final Office Action dated April 27, 2006 is being appealed.

VIII. APPELLANT'S ARGUMENTS

Applicants respectfully submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features recited in any of the pending claims, at least for the reasons discussed below.

The Final Office Action rejected claims 1-60 under 35 U.S.C. 103(a) as being obvious over US Patent No. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), further in view of US Patent No. 5,860,136 to Fenner (Fenner), further in view of US Patent No, 6,614,796 to Black et al. (Black). The Office Action took the position that Muller taught all the elements of the claims 1-60, except for a single buffer per packet mechanism, an index key and the key being a portion of the destination address. Steiner was cited as providing the single buffer per packet mechanism. Fenner was cited as providing the index key, and Black was cited as providing the key being a predefined portion of the destination address. Applicants respectfully submit that the cited references, either alone or in combination, fail to

disclose or suggest all the features of any of the presently pending claims.

1. Independent Claims 1, 8, 13, 28, 32, 52 and 57

Claims 1, 8, 13, 28, 32, 52 and 57 are summarized above.

As discussed in the specification, examples of the present invention enable a memory structure to resolve addresses in a packet-based network switch. Exemplary embodiments of the present invention enable bandwidth savings that are attributed to a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table. Applicant respectfully submits that the cited references of Muller, Steiner, Fenner, and Block, when viewed alone or combined, fail to disclose or suggest all the elements of the presently pending claims and further, the use of four references in an indication of inappropriateness of the rejection. Therefore, the cited references fail to provide the critical and unobvious advantages discussed above.

Muller relates to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager

220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

Steiner relates to prioritized-buffer management for fixed size packets in a multimedia application. Steiner describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. Steiner also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. Steiner also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Fenner relates to a method and apparatus for use of associated memory with large key spaces. Fenner describes an associative memory that utilizes a location addressable memory and a lookup table to generate, from a key, the address in memory storing an associated record. Fenner describes an associative memory utilizing arithmetic coding to associate a key presented to the memory with a record stored in the memory. The associative memory includes an index table stored in memory and a record memory for storing the records of data. The index table is constructed so that each symbol of a key, with a key being divided into a string of symbols and each symbol being defined by its position within the key and its value, addresses an index value in the index

table memory. The index values are assigned such that the sum of index values for a given key is a unique value that is used to address the record memory.

Black is directed to transferring data through a Fibre Channel Arbitrated Loop (FCAL) switch. The FCAL switch uses multiple switch control circuits each coupled to one FCAL network, all of which are connected to a crossbar switch. The destination of each OPN is used to address a lookup table in each switch control circuit to determine if the destination node is local.

Applicants respectfully submit that the Final Office Action failed to establish *prima facie* obviousness in rejecting claims 1, 8, 13, 28, 32, 52 and 57 of the present application. Applicants respectfully submit that 1) the Final Office Action applied impermissible hindsight reasoning and piecemeal analysis in citing four references to recreate the Applicant's invention, and 2) the cited references taken individually or in combination, fail to disclose or suggest all of the features recited in any of the pending claims.

To establish *prima facie* obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). There are three possible sources for a motivation to combine references: the nature of the problem

to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

Applicants respectfully submit that one skilled in the art would not be motivated to combine the teachings of the cited references as alleged in the Final Office Action. Specifically, Applicants respectfully submit that the Office Action applied piecemeal analysis and improper hindsight reasoning in forming the basis to reject claims 1, 8, 13, 28, 32, 52 and 57.

Furthermore, as noted above, it is well-established in United States patent law that a piecemeal analysis of a number of references, to extract a number of individual elements which are picked and chosen to recreate the claimed invention, is improper absent some teaching or suggestion in the references to support their use in the particular claimed combination. It is further improper to look to the Applicant's own disclosure for any such motivation or incentive. Interconnect Planning Corporation v. Feil, 227 USPQ 543 (Fed. Cir. 1985), Symbol Technologies Inc. v. Opticon, Inc., 19 USPQ 2d. 1241 (Fed. Cir. 1991), In re Rothermel and Waddel, 125 USPQ 328 (CCPA 1960), In re Jones, 21 USPQ 2d. 1941 (Fed. Cir. 1992).

In the present case, Applicants respectfully submit that the Office Action's use of four references to form the basis for rejecting the pending claims, is an indication of piecemeal reconstruction of the Applicants' invention. Thus, there is no motivation, either in the references themselves or in knowledge of one skilled in the art to combine the teaching of these references. This is further evidence of the non-obviousness of the present invention. As stated above, the final Office Action asserted that this feature "if

not directly taught by Black, and if not reasonably implied by Black through teachings of efficiency (see Black, col. 8 lines 10-32) or through teaching a search key that is distinct from the destination address (see col. 8 lines 54-55), using a predefined portion of the destination address in Black instead of using the entire destination address would have been obvious to one of ordinary skill in the art at the time of the invention in order to conserve a variety of system resources known in the art." There is no motivation either through one skilled in the art or in any of Muller, Steiner and Fenner to add the teachings of Black as a fourth reference to allegedly disclose or suggest an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address, outside of impermissible hindsight reasoning to reconstruct the Applicants' invention. Thus, as previously argued, not only does Black fail to cure the admitted deficiencies of Muller, Steiner and Fenner, the inclusion thereof is the result of improper hindsight reasoning and piecemeal analysis, because the only motivation to do so, is obtained from the Applicants' disclosure.

Further, Applicants respectfully submit that the cited references, taken individually or in combination, fail to disclose or suggest all of the features of the above claims because Black fails to cure the admitted deficiencies of Muller, Steiner and Fenner, for the reasons set forth below. Thus, *prima facie* obviousness is not established in the Final Office Action because the cited references fail to disclose or suggest all of the features recited in claims 1, 8, 13, 28, 32, 52 and 57.

Specifically, the cited combination of references fail to disclose or suggest at least the feature of an Address Resolution Table for resolving addresses in a packet-based

network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address, as recited in claims 1, 8, 13, 28, 32, 52 and 57. The Office Action alleged that Black disclosed this feature in col. 8 lines 54-58 of Black. However, Applicants respectfully submit that Black fails to cure the admitted deficiencies of Muller, Steiner and Fenner.

Applicants respectfully submit that Black merely discloses using the destination address in the OPN primitive as a search key. Nowhere does Black disclose or suggest using a predefined portion of the destination address as a key to search a routing table, as recited in the pending claims. Thus, Black fails to cure the admitted deficiencies of Muller, Steiner and Fenner.

In the "Response to Arguments" section, the Final Office Action asserted that even if this feature "if not directly taught by Black, and if not reasonably implied by Black through teachings of efficiency (see Black, col. 8 lines 10-32) or through teaching a search key that is distinct from the destination address (see col. 8 lines 54-55), using a predefined portion of the destination address in Black instead of using the entire destination address would have been obvious to one of ordinary skill in the art at the time of the invention in order to conserve a variety of system resources known in the art."

Applicant respectfully disagrees for the following reasons. The cited portion of Black (col. 8 lines 54-55) does not even mention, let alone disclose or suggest, that "a search key that is distinct from the destination address" as alleged in the Office Action. Instead, the section merely discusses the use of the destination address as a search key as one embodiment of the invention ("using the destination address in the OPN primitive as a search key . . ."). Black goes no further to disclose or suggest that a "pre-defined

portion" of the destination address is used as a search key. Thus, the Office Action's argument that Black implies or renders obvious that a predefined portion of the destination address is used as a search key, improperly adds features to Black that are neither reasonably implied, nor inherent to the teachings of Black.

Thus, based at least on the above, Black fails to cure the admitted deficiencies of Muller, Steiner and Fenner. Accordingly, the cited references fail to disclose or suggest all of the features recited in claims 1, 8, 13, 28, 32, 52 and 57.

Regarding dependent claims 2-7, 9-12, 14-27, 29-31, 33-51, 53-56 and 58-60, Applicants respectfully submit that Muller, Steiner, Fenner and Black, are deficient at least for the same reasons discussed above regarding claims 1, 8, 13, 28, 32, 52 and 57, as well as for the additional features recited in these dependent claims.

2. Claim 2.

Claim 2, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 2 are neither disclosed nor suggested in the cited references taken individually or in combination.

3. Claim 3

Claim 3, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 3 are neither disclosed nor suggested in the cited references taken individually or in combination.

4. Claim 4

Claim 4, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 4 are neither disclosed nor suggested in the cited references taken individually or in combination.

5. Claim 5

Claim 5, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 5 are neither disclosed nor suggested in the cited references taken individually or in combination.

6. Claim 6

Claim 6, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 6 are neither disclosed nor suggested in the cited references taken individually or in combination.

7. Claim 7

Claim 7, depends from claim 1 and recites additional features. It is respectfully submitted that the features recited in claim 7 are neither disclosed nor suggested in the cited references taken individually or in combination.

8. Claim 9

Claim 9, depends from claim 8 and recites additional features. It is respectfully submitted that the features recited in claim 9 are neither disclosed nor suggested in the cited references taken individually or in combination.

9. Claim 10

Claim 10, depends from claim 8 and recites additional features. It is respectfully submitted that the features recited in claim 10 are neither disclosed nor suggested in the cited references taken individually or in combination.

10. Claim 11

Claim 11, depends from claim 8 and recites additional features. It is respectfully submitted that the features recited in claim 11 are neither disclosed nor suggested in the

cited references taken individually or in combination.

11. Claim 12

Claim 12, depends from claim 8 and recites additional features. It is respectfully submitted that the features recited in claim 8 are neither disclosed nor suggested in the cited references taken individually or in combination.

12. Claim 14

Claim 14, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 14 are neither disclosed nor suggested in the cited references taken individually or in combination.

13. Claim 15

Claim 15, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 15 are neither disclosed nor suggested in the cited references taken individually or in combination.

14. Claim 16

Claim 16, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 16 are neither disclosed nor suggested in the cited references taken individually or in combination.

15. Claim 17

Claim 17, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 17 are neither disclosed nor suggested in the cited references taken individually or in combination.

16. Claim 18

Claim 18, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 18 are neither disclosed nor suggested in the cited references taken individually or in combination.

17. Claim 19

Claim 19, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 19 are neither disclosed nor suggested in the cited references taken individually or in combination.

18. Claim 20

Claim 20, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 20 are neither disclosed nor suggested in the cited references taken individually or in combination.

19. Claim 21

Claim 21, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 21 are neither disclosed nor suggested in the cited references taken individually or in combination.

20. Claim 22

Claim 22, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 22 are neither disclosed nor suggested in the cited references taken individually or in combination.

21. Claim 23

Claim 23, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 23 are neither disclosed nor suggested in the cited references taken individually or in combination.

22. Claim 24

Claim 24, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 24 are neither disclosed nor suggested in the cited references taken individually or in combination.

23. Claim 25

Claim 25, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 25 are neither disclosed nor suggested in the cited references taken individually or in combination.

24. Claim 26

Claim 26, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 26 are neither disclosed nor suggested in the cited references taken individually or in combination.

25. Claim 27

Claim 27, depends from claim 13 and recites additional features. It is respectfully submitted that the features recited in claim 27 are neither disclosed nor suggested in the cited references taken individually or in combination.

26. Claim 29

Claim 29, depends from claim 28 and recites additional features. It is respectfully submitted that the features recited in claim 29 are neither disclosed nor suggested in the cited references taken individually or in combination.

27. Claim 30

Claim 30, depends from claim 28 and recites additional features. It is respectfully submitted that the features recited in claim 30 are neither disclosed nor suggested in the

cited references taken individually or in combination.

28. Claim 31

Claim 31, depends from claim 28 and recites additional features. It is respectfully submitted that the features recited in claim 31 are neither disclosed nor suggested in the cited references taken individually or in combination.

29. Claim 33

Claim 33, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 33 are neither disclosed nor suggested in the cited references taken individually or in combination.

30. Claim 34

Claim 34, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 34 are neither disclosed nor suggested in the cited references taken individually or in combination.

31. Claim 35

Claim 35, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 35 are neither disclosed nor suggested in the cited references taken individually or in combination.

32. Claim 36

Claim 36, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 36 are neither disclosed nor suggested in the cited references taken individually or in combination.

33. Claim 37

Claim 37, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 37 are neither disclosed nor suggested in the cited references taken individually or in combination.

34. Claim 38

Claim 38, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 38 are neither disclosed nor suggested in the cited references taken individually or in combination.

35. Claim 39

Claim 39, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 39 are neither disclosed nor suggested in the cited references taken individually or in combination.

36. Claim 40

Claim 40, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 40 are neither disclosed nor suggested in the cited references taken individually or in combination.

37. Claim 41

Claim 41, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 41 are neither disclosed nor suggested in the cited references taken individually or in combination.

38. Claim 42

Claim 42, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 42 are neither disclosed nor suggested in the cited references taken individually or in combination.

39. Claim 43

Claim 43, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 43 are neither disclosed nor suggested in the cited references taken individually or in combination.

40. Claim 44

Claim 44, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 44 are neither disclosed nor suggested in the cited references taken individually or in combination.

41. Claim 45

Claim 45, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 45 are neither disclosed nor suggested in the cited references taken individually or in combination.

42. Claim 46

Claim 46, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 46 are neither disclosed nor suggested in the cited references taken individually or in combination.

43. Claim 47

Claim 47, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 47 are neither disclosed nor suggested in the cited references taken individually or in combination.

44. Claim 48

Claim 48, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 48 are neither disclosed nor suggested in the

cited references taken individually or in combination.

45. Claim 49

Claim 49, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 49 are neither disclosed nor suggested in the cited references taken individually or in combination.

46. Claim 50

Claim 50, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 50 are neither disclosed nor suggested in the cited references taken individually or in combination.

47. Claim 51

Claim 51, depends from claim 32 and recites additional features. It is respectfully submitted that the features recited in claim 51 are neither disclosed nor suggested in the cited references taken individually or in combination.

48. Claim 53

Claim 53, depends from claim 52 and recites additional features. It is respectfully submitted that the features recited in claim 53 are neither disclosed nor suggested in the cited references taken individually or in combination.

49. Claim 54

Claim 54, depends from claim 52 and recites additional features. It is respectfully submitted that the features recited in claim 54 are neither disclosed nor suggested in the cited references taken individually or in combination.

50. Claim 55

Claim 55, depends from claim 52 and recites additional features. It is respectfully submitted that the features recited in claim 55 are neither disclosed nor suggested in the cited references taken individually or in combination.

51. Claim 56

Claim 56, depends from claim 52 and recites additional features. It is respectfully submitted that the features recited in claim 56 are neither disclosed nor suggested in the cited references taken individually or in combination.

52. Claim 58

Claim 58, depends from claim 57 and recites additional features. It is respectfully submitted that the features recited in claim 58 are neither disclosed nor suggested in the cited references taken individually or in combination.

53. Claim 59

Claim 59, depends from claim 57 and recites additional features. It is respectfully submitted that the features recited in claim 59 are neither disclosed nor suggested in the cited references taken individually or in combination.

55. Claim 60

Claim 60, depends from claim 57 and recites additional features. It is respectfully submitted that the features recited in claim 60 are neither disclosed nor suggested in the cited references taken individually or in combination.

Based at least on the above, Applicants respectfully submit that the cited references, taken individually or in combination, fail to disclose or suggest all of the features recited in any of claims 1-60, and therefore, the Final Office Action failed to establish *prima facie* obviousness in rejecting claims 1-60. Accordingly, withdrawal of the

rejection of claims 1-60 under 35 U.S.C. 103(a) is respectfully requested.

IX. CONCLUSION

For all of the above noted reasons, it is strongly contended that certain clear differences exist between the present invention as claimed in claims 1-60 and the prior art relied upon by the Examiner. It is further contended that these differences are more than sufficient that the present invention would not have been obvious to a person having ordinary skill in the art at the time the invention was made.

This final rejection being in error, therefore, it is respectfully requested that this honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of application claims 1-60.

In the event that this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Encls: Appendix 1 – Claims on Appeal
Appendix 2 – Related Proceedings
Appendix 3 – Evidence
Appendix 4 – Drawings of Application Serial No. 09/492,265

APPENDIX 1

CLAIMS ON APPEAL

1. (Previously Presented) A memory structure, comprising:

an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table, wherein the key is a predefined portion of a packet destination address;

a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table; and

a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted.

2. (Previously Presented) The memory structure of claim 1, further comprising at least one of:

a Transmit Descriptor Table being associated with a corresponding packet-based network transmit port; and

a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

3. (Previously Presented) The memory structure of claim 1 wherein the packet-based network switch implements an IEEE standard 802.3 communication

protocol.

4. (Previously Presented) The memory structure of claim 3 wherein the switch comprises plural ports.

5. (Previously Presented) The memory structure of claim 4 wherein the switch comprises at least 8 ports.

6. (Previously Presented) The memory structure of claim 1 wherein an associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

7. (Previously Presented) The memory structure of claim 3 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

8. (Previously Presented) A memory structure comprising an Address Resolution Table having an associative memory structure, the Address Resolution Table for

resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table, and a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted, wherein the key is a predefined portion of a packet destination address.

9. (Previously Presented) The memory structure of claim 8 further comprising a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

10. (Previously Presented) The memory structure of claim 9 further comprising a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value.

11. (Previously Presented) The memory structure of claim 8 wherein the associative memory structure comprises one of a direct-mapped/one-way associative memory structure and a two-way associative memory structure.

12. (Previously Presented) The memory structure of claim 11 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

13. (Previously Presented) A memory structure having a memory block, the memory block comprising:

an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table, wherein the key is a predefined portion of a packet destination address;

a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value;

a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion; and

a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted.

14. (Previously Presented) The memory structure of claim 13 wherein the

associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

15. (Previously Presented) The memory structure of claim 13 wherein the memory block comprises a shared memory block.

16. (Previously Presented) The memory structure of claim 13 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

17. (Previously Presented) The memory structure of claim 16 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and tail memory pointer.

18. (Previously Presented) The memory structure of claim 13 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

19. (Previously Presented) The memory structure of claim 18, wherein the Free Buffer Pool further comprises a buffer control memory.

20. (Previously Presented) The memory structure of claim 19, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory

locations.

21. (Previously Presented) The memory structure of claim 18, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

22. (Previously Presented) The memory structure of claim 21 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

23. (Previously Presented) The memory structure of claim 18, further comprising a free buffer manager, including:

a buffer bus controller;

a buffer bus register;

a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

24. (Previously Presented) The memory structure of claim 23 wherein the buffer bus controller comprises:

a buffer free bus controller for detecting a buffer request and presenting the request to at least one of the finite state machine and the buffer search engine; and

a buffer grant bus controller for granting an available free buffer, as indicated by the buffer, as indicated by the buffer bus register.

25. (Previously Presented) The memory structure of claim 23 wherein the buffer search engine comprises a pipelined buffer search engine.

26. (Previously Presented) The memory structure of claim 23 wherein the buffer bus register comprises a LIFO.

27. (Previously Presented) The memory structure of claim 26 wherein the LIFO comprises an eight-location LIFO.

28. (Currently Amended) A packet-based switch comprising a shared memory structure having an Address Resolution Table and a Packet Storage Table, a key to index a location within the Address Resolution Table, and a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit

descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the key is a predefined portion of a packet destination address, and wherein the entire packet is to be transmitted.

29. (Previously Presented) The packet-based switch of claim 28 wherein the switch implements an IEEE Standard 802.3 communication protocol.

30. (Previously Presented) The packet-based switch of claim 29 wherein the switch comprises plural ports.

31. (Previously Presented) The packet-based switch of claim 28 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

32. (Previously Presented) A packet-based switch having a memory structure, the memory structure comprising:

an Address Resolution Table having an associative memory structure, the

Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location with the Address Resolution Table, wherein the key is a predefined portion of a packet destination address;

a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value;

a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion; and

a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted.

33. (Previously Presented) The packet-based switch of claim 32, wherein the associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

34. (Previously Presented) The packet-based switch of claim 32 wherein the memory block comprises a shared memory block.

35. (Previously Presented) The packet-based switch of claim 32 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

36. (Previously Presented) The packet-based switch of claim 35 wherein the FIFO memory structure comprises a circular FIFO memory structure the FIFO memory structure having a head memory pointer and a tail memory pointer.

37. (Previously Presented) The packet-based switch of claim 32 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

38. (Previously Presented) The packet-based switch of claim 37, wherein the Free Buffer Pool further comprises a buffer control memory.

39. (Previously Presented) The packet-based switch of claim 38, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the predetermined number of buffer pool memory locations.

40. (Previously Presented) The packet-based switch of claim 37, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

41. (Previously Presented) The packet-based switch of claim 34 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one

of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and'

one cycle per eight bytes for a frame data write.

42. (Previously Presented) The packet-based switch of claim 38, further comprising a free buffer manager, including:

a buffer bus controller;

a buffer bus register;

a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

43. (Previously Presented) The packet-based switch of claim 42 wherein the buffer bus controller comprises:

a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and

a buffer grant bus controller for granting an unavailable free buffer, as indicated by the buffer bus register.

44. (Previously Presented) The packet-based switch of claim 42 wherein the buffer search engine comprises a pipelined buffer search engine.

45. (Previously Presented) The packet-based switch of claim 42 wherein the buffer bus register comprises a LIFO.

46. (Previously Presented) The packet-based switch of claim 45 wherein the LIFO comprises an eight-location LIFO.

47. (Previously Presented) The packet-based switch of claim 33 wherein the switch implements an IEEE Standard 802.3 communication protocol.

48. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises plural ports.

49. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises at least 4 ports.

50. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises at least 8 ports.

51. (Previously Presented) The packet-based switch of claim 45 wherein a

packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

52. (Previously Presented) A packet-based switch comprising an Address Resolution Table having a one-way associative memory structure and using a key to index a location within the Address Resolution Table, and a Packet Data Buffer Table sharing a memory block with an Address Resolution Table, and a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the key is a predefined portion of a packet destination address, wherein the entire packet is to be transmitted.

53. (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises plural ports.

54. (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises at least 4 ports.

55. (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises at least 8 ports.

56. (Previously Presented) The packet-based switch of claim 52 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

57. (Previously Presented) A packet-based switch, comprising an Address Resolution Table having a direct-mapped/one-way associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch, a key to index a location within the Address Resolution Table, and a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a

single access in order to locate an entire packet at the location using the key, wherein the key is a predefined portion of a packet destination address, wherein the entire packet is to be transmitted.

58. (Previously Presented) The packet-based switch of claim 57 wherein the direct-mapped/one-way associative memory is searched using a destination address key direct-mapped address search.

59. (Previously Presented) The packet-based switch of claim 58 wherein the switch implements an IEEE Standard 802.3 communication protocol.

60. (Previously Presented) The packet-based switch of claim 59, wherein the switch comprises plural ports.

APPENDIX 2

EVIDENCE APPENDIX

No evidence under section 37 C.F.R. 1.130, 1.131, or 1.132 has been entered or will be relied upon by Appellants in this appeal.

APPENDIX 3

RELATED PROCEEDINGS APPENDIX

No decisions of the Board or of any court have been identified under 37 C.F.R. §41.37(c)(1)(ii).

APPENDIX 4

DRAWINGS OF APPLICATION SERIAL NO. 09/492,265

The drawings of U.S. Application No. 09/492,265 are attached.

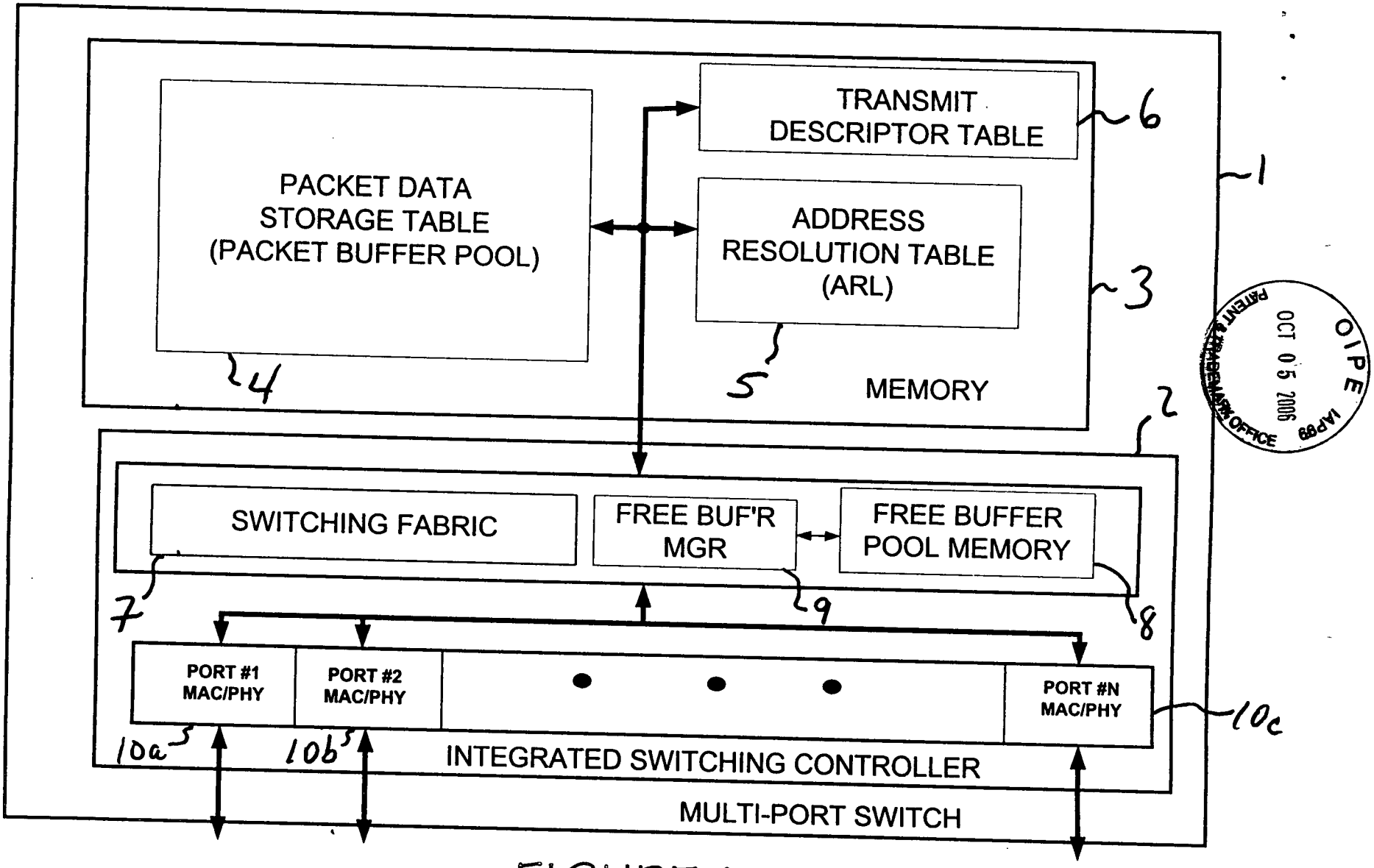


FIGURE 1

Address[7:0]	Data[63:0]
00-CF	Packet Data
D0	Port 0 Transmit Descriptor
D1	Port 1 Transmit Descriptor
D2	Port 2 Transmit Descriptor
D3	Port 3 Transmit Descriptor
D4	Port 4 Transmit Descriptor
D5	Port 5 Transmit Descriptor
D6	Port 6 Transmit Descriptor
D7	Port 7 Transmit Descriptor
D8	Port 8 Transmit Descriptor
D9-DF	Unused
E0-FF	32 ARL Table Entries

11 12 13 14 15 16 17 18 100

FIGURE 2

Address[16:0]	Data[63:0]
0000-00FF	Memory Block 0
0100-01FF	Memory Block 1
0200-02FF	Memory Block 2
0300-FEFF	Memory Block 3 to 2046
FF00-FFFF	Memory Block 2047
10000-1FFFF	Optional Memory Block 2048-4095

19 20

FIGURE 3

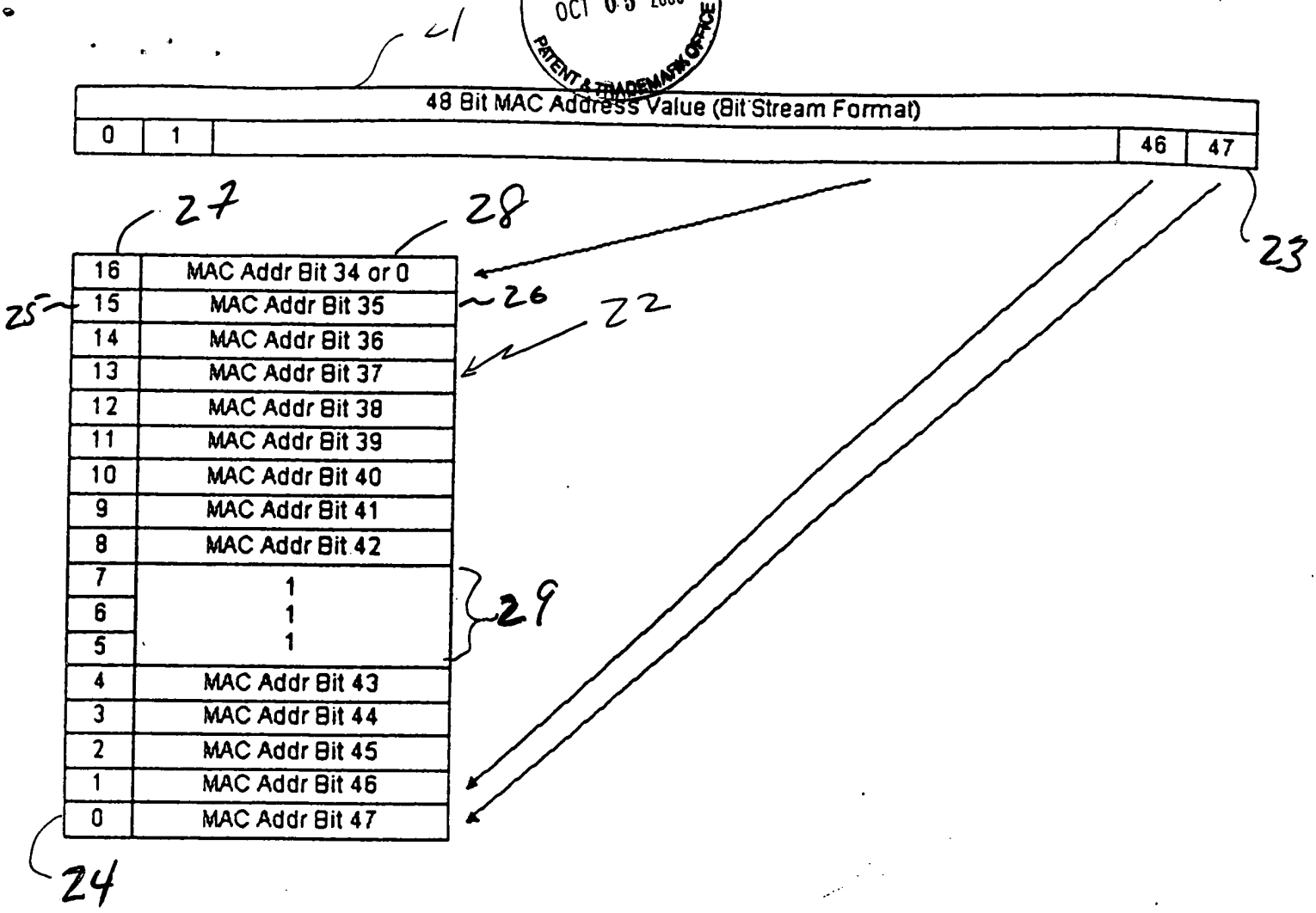


FIGURE 4

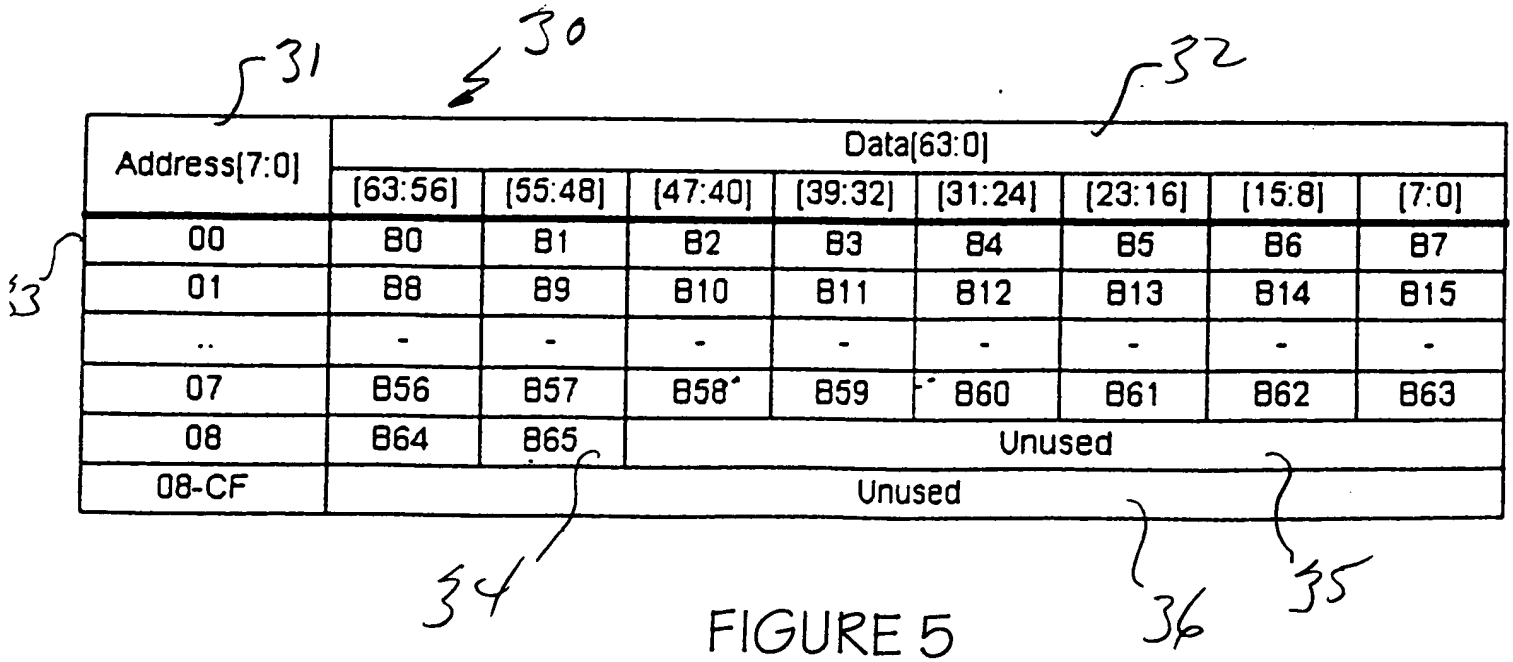


FIGURE 5

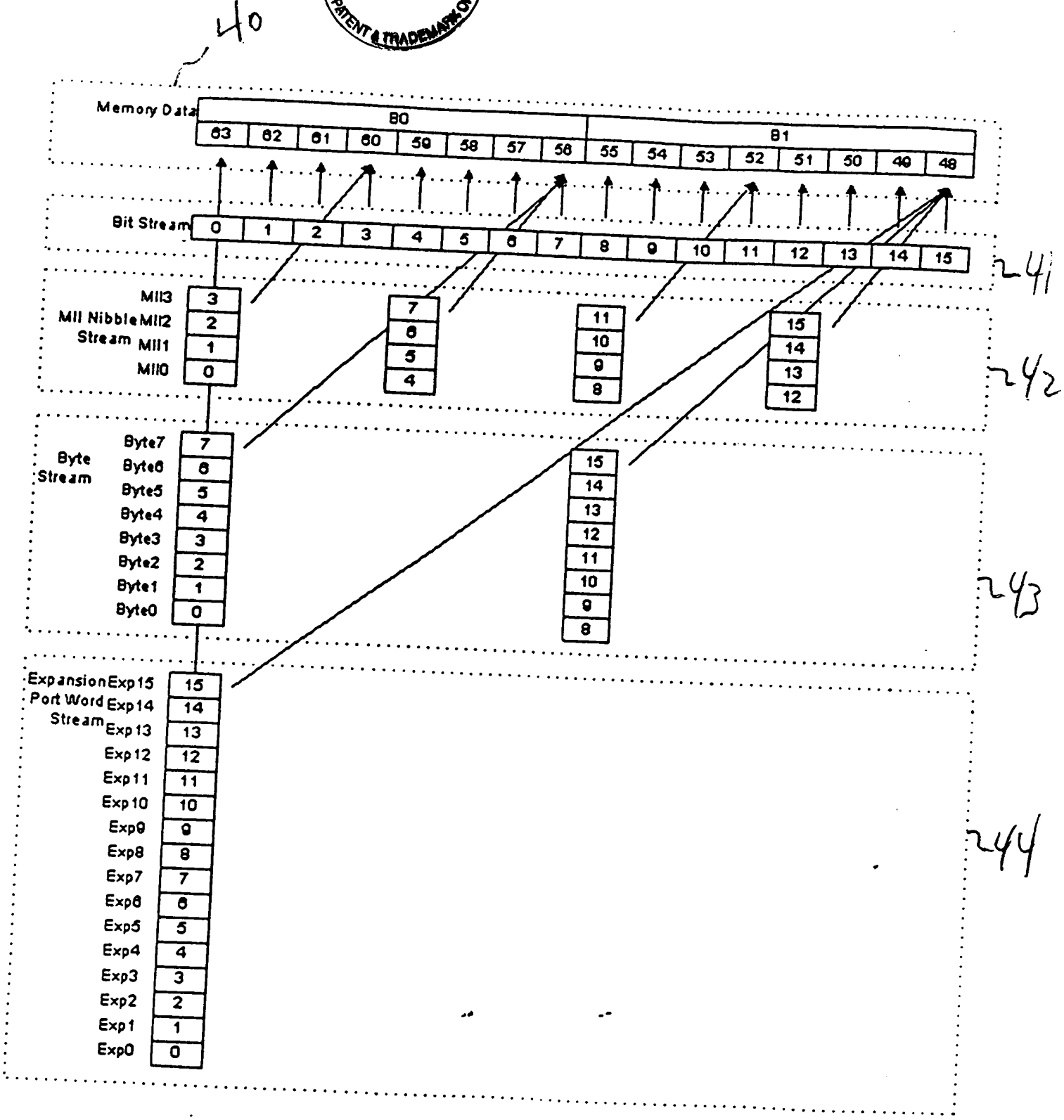
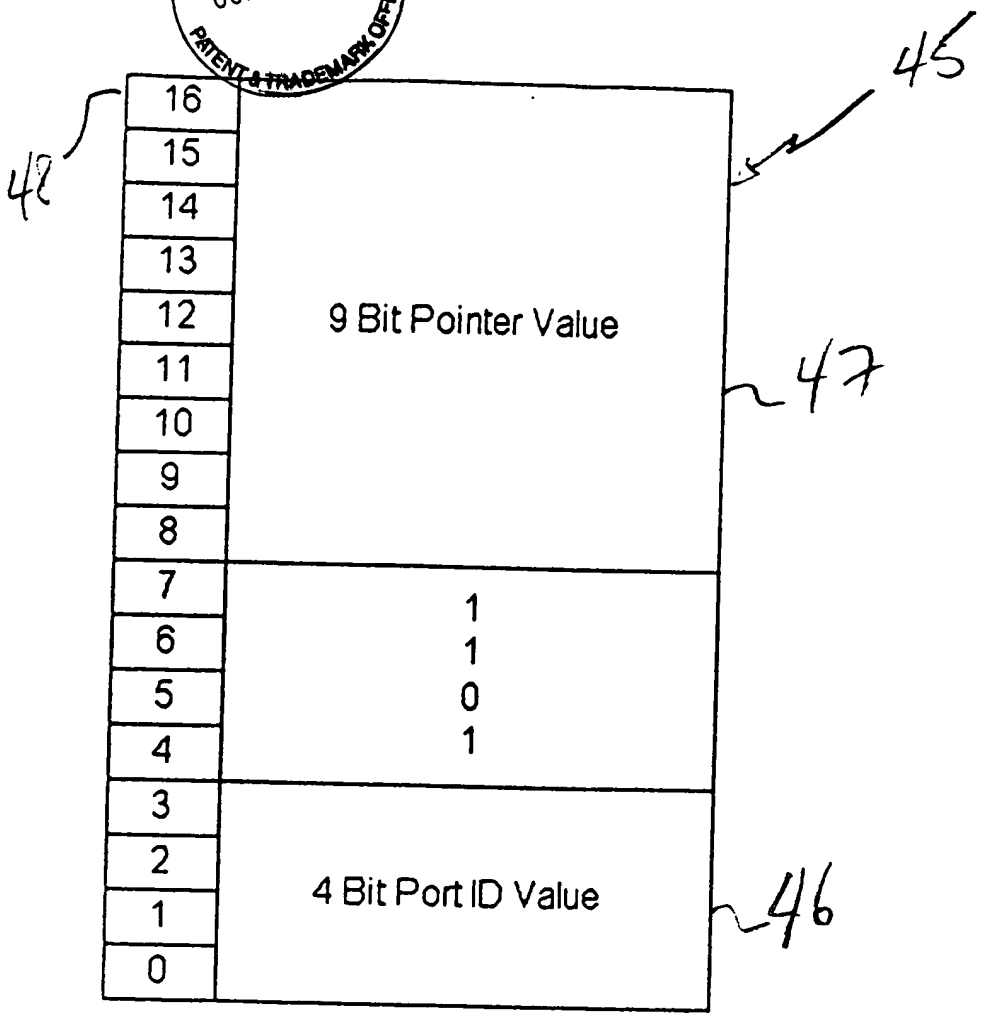


FIGURE 6



Transmit Descriptor Pointer Address

FIGURE 7

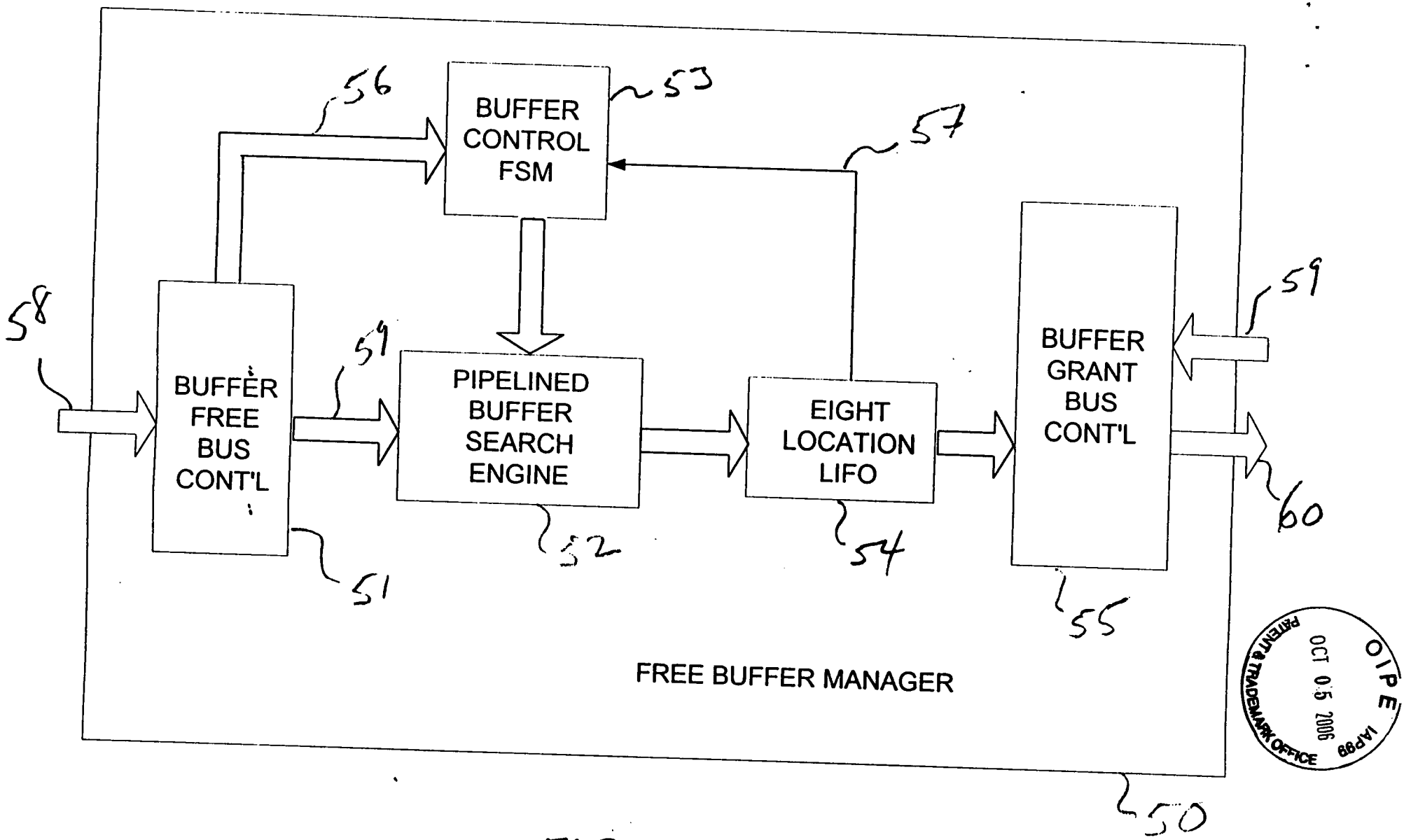


FIGURE 8

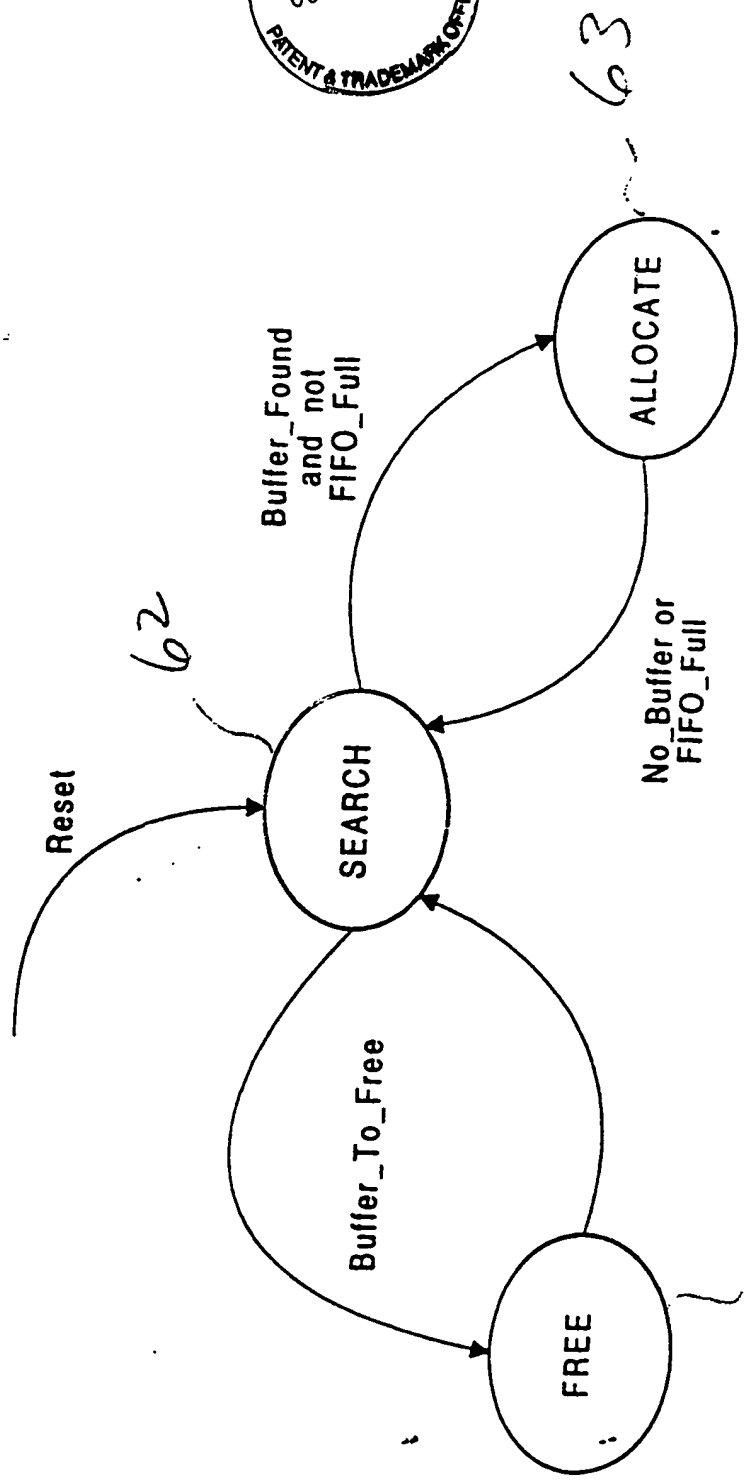


FIGURE 9